Abstract of the Disclosure

A method of fabricating a high performance capacitor that may be incorporated into a standard CMOS fabrication process suitable for submicron devices is described. The parameters used in the standard CMOS process may be maintained, particularly for the definition and etch of the lower electrode layer. To reduce variation in critical dimension width, an Anti-Reflective Layer (ARL) is used. In the preferred embodiment, this is of the Plasma Enhanced chemical vapor deposition Anti-Reflective Layer (PEARL) type, although other Anti-Reflective Coatings (ARCs) or layers, such as a conductive film like TiN may be employed. This ARL formation occurs after the capacitor specific process steps, but prior to the masking used for defining the lower electrodes. In one embodiment, a Rapid Thermal Oxidation (RTO) is performed subsequent to removing the unwanted capacitor dielectric layer from the transistor poly outside of the capacitor regions, but prior to the PEARL deposition. Another embodiment instead eliminates the capacitor dielectric removal step, which is then replaced by a step to form an additional layer which, in a second step, is then etched away to leave spacers on the capacitor sides, thereby eliminating any undercutting of the dielectric.